IN THE CLAIMS

Please amend the claims as follows:

Claims 1-29 (Canceled).

Claims 30 (New) A semiconductor memory device comprising:

a first wiring extending in a first direction;

a second wiring extending in a second direction differing from said first direction;

a magneto resistive element arranged between said first wiring and said second wiring, said magneto resistive element having a magnetically fixed layer, a magnetic recording layer and a tunnel barrier wall layer interposed between said magnetically fixed layer and said magnetic recording layer, said magnetic recording layer being in contact with said second wiring and said magnetic recording layer extending along said second wiring from an inside region to an outside region, over a plurality of cells; and

a metal layer in contact with said magnetically fixed layer and arranged apart from said first wiring.

Claim 31 (New) The semiconductor memory device according to claim 30, further comprising a constricted portion formed in the outside region,

wherein said magnetic recording layer and said second wiring of said outside region are narrower in said constricted portion than said second wiring and said magnetic recording layer of said inside region.

Claim 32 (New) The semiconductor memory device according to claim 30, further comprising a folded portion formed in the outside region,

wherein said magnetic recording layer and said second wiring are bent in a direction differing from said second direction in said folded portion.

Claim 33 (New) The semiconductor memory device according to claim 30, further comprising at least one of a transistor and a diode connected to said metal layer.

Claim 34 (New) The semiconductor memory device according to claim 30, wherein a portion of said magnetic recording layer extends along said second wiring from said inside portion to said outside portion, over said plurality of cells.

Claim 35 (New) The semiconductor memory device according to claim 30, wherein said tunnel barrier wall layer extends along said magnetic recording layer and said second wiring from said inside region to said outside region, over said plurality of cells.